Claims:

1. An apparatus for processing tokens having variable length, comprising:

a padder to receive the tokens and to pad a portion of the tokens received by adding a tail which produces new tokens having integer numbers of data words of a predetermined length; and

a storage buffer configured to store data words of the predetermined length and coupled to receive the new data tokens from the padder.

2. The apparatus of claim 1, wherein two types of the new tokens have two different numbers of words.

3. The apparatus of claim 1, wherein different data tokens may have different numbers of data words.

4. The apparatus of claim 1, further comprising:

a multi-stage pipelined decoder; and

a two-wire interface coupling the pipeline to an output of the buffer.

5. The apparatus of claim 4, wherein a portion of the stages of the decoder are reconfigurable to decode video data by a portion of the tokens.

6. The apparatus of claim 5, wherein configurations of the stages are responsive to standards by which data in the portion of the tokens is formatted.

7. The apparatus of claim 6 wherein the standards include two of MPEG, JPEG, and H.261.

8. The apparatus of claim 1, further comprising:
a start code detector, the buffer being located in the start code detector.

9. The apparatus of claim 1, further comprising:
a semiconductor chip, the padder and the buffer being located on the chip.

10. The apparatus of claim 1, wherein the padder is a hardware device.

11. The apparatus of claim 4, wherein the pipeline includes:
a Huffman decoder coupled to receive the tokens from the padder;
a token formatter coupled to receive data from the Huffman decoder; and
an inverse modeler coupled to receive data from the token formatter.

12. A method of processing video data, comprising:
receiving tokens in a first stage of a pipeline, a portion of the tokens having a plurality of words;
padding one of the tokens to have a length equal to an integral number of words;
sending the tokens to the remainder of the pipeline; and

reconfiguring a portion of the stages of the remainder of the pipeline for data processing in response to receiving the tokens belonging to predetermined token types.

13. The method of claim 12, wherein reconfiguring is responsive to standards by which video data in the received tokens are formatted.

14. The method of claim 13, wherein the standards include two of MPEG, JPEG, and H.261.

15. The method of claim 12, further comprising:
detecting a start code in a data stream; and
wherein padding is performed in response to detecting the start code.

16. The method of claim 12, wherein each word of a token includes one or more extension bits.

17. The method of claim 16, wherein reconfiguring one of the stages includes:
receiving a first word of one of the tokens in the one of the stages; and
reconfiguring the one of the stages to process the word in response to determining that the first word belongs to a type of token processed by the one of the stages.

18. The method of claim 17, further comprising:
receiving another word in the one of the stages; and

reading one or more extension bits of the other word and processing the other word according to the procedure for processing a previous word in response to determining that the other word belongs to a same token as the previous word.

19. A system for decoding video frames, comprising:

a token padder to pad data tokens of different lengths by adding a tail which produces new tokens having integer numbers of data words of a predetermined length;

a Huffman decoder to receive the padded tokens;

a token formatter coupled to receive data tokens from the Huffman decoder;

a buffer to store tokens from the token formatter; and

an inverse modeler coupled to receive the tokens from the buffer.

20. The system of claim 19, wherein the Huffman decoder is configured to decode data of at least two of the standards JPEG, MPEG, and H.261.

21. The system of claim 19 further comprising:

an inverse quantizer coupled to receive data from the inverse modeler; and

an inverse discrete cosine transformer coupled to the inverse quantizer.

22. The system of claim 19, wherein the decoder is a hardware device.